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Towards Expressive Specification and Efficient Model Checking

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System modeling is important and highly non-trivial. The choice of specification language is an important factor in the success of the entire development. The language should cover several facets of the requirements and the model should precisely capture (up to abstraction of irrelevant details) an existing system or a system to be built. The language should have a semantic model suitable to study the behaviors of the system and to establish the validity of desired properties. A formal model can be the basis for a variety of system development activities, e.g., system simulation, visualization, verification or prototype synthesis.

In general, specifications are not necessarily executable [2]. Over the last decade, expressiveness is the main driving force in the specification language research community. Many integrated formal specification languages have been proposed in order to model systems with not only complicated control flows but also complex data structures and operations. Examples include Circus [6] and TCOZ [3]. However the downside of the high expressitiveness is that it is extremely difficult to develop automatic reasoning tools for those languages. On the other hand, popular model checkers like SPIN, SMV and FDR are designed for specialized domains and are therefore based on restrictive modeling languages. For instance, Promela (supported by SPIN) is based on a subset of CSP for communicating network protocols. The input language of SMV is initially designed for specification of hardware circuits. A number of compositional operators which model common system behavior patterns are missing in both languages. FDR, which supports all operators of CSP, however, lacks support of shared variables or non-trivial data-types. Language limitations can be significant barrier to the practical verification of complex systems.

We share the views that specifications are preferably executable [1]. In this tutorial, we introduce our latest effort on combining the expressiveness of integrated formal specification languages with the power of mechanical system analysis method like model checking. We present a process analysis toolkit (PAT [4, 5], available at http://pat.comp.nus.edu.sg), which is a self-contained framework for system specification, simulation and verification. PAT supports a modeling language named CSP# (short for communicating sequential proJun Sun National University of Singapore sunj@comp.nus.edu.sg

grams), which shares similar design principle with specification languages like TCOZ. Nonetheless, instead of relying on the Z language, CSP# mixes high-level modeling operators with low-level programs, for the purpose of flexible system modeling and efficient verification. In CSP#, data operations can be modeled as terminating sequential programs, which then can be composed using high-level compositional operators. *The idea is to treat sequential terminating programs, which may indeed be C# programs, as internal events.* The result is a highly expressive modeling language which covers many application domains.

CSP# models are executable with complete operational semantics, and therefore subject to fully automated system verification techniques like model checking. PAT verifies CSP# models using state-of-art model checking techniques, e.g., on-the-fly explicit state model checking with partial order reduction. Besides new modeling techniques, PAT complements existing model checkers in a number of aspects. For instance, it supports an assertion language which allows LTL formulae constituted with propositions and events. It has dedicated algorithms for model checking under a variety of fairness constraints, which are often required for verification of liveness properties. CSP# and PAT have been applied a many systems including distributed algorithms, concurrent data objects, parameterized systems, etc. Previously unknown bugs have been identified.

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